Exhibit 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner,

Case No. IPR2022-00615

Patent No. 7,619,912

REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF

ANDREW WOLFE, PH.D.

WEDNESDAY, JANUARY 4, 2023

Reported by:

Ashala Tylor, CSR #2436, CLR, CRR, RPR

JOB NO. 5621734

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wanted to build a x64 module, then you would do that. The other example is when four 32Mbx16 chips is cheaper than two 64Mbx16 chips or more readily available, you might do it in that situation as well. 12:09

Q. And reason number one, you are assuming a x64 memory module as well as all four of the DRAM devices would be used in one rank; is that correct? 12:10

A. In that particular situation, yes. 12:10

Q. So what if you are using a x16 memory module width and you are trying to build a 2-gigabit memory -- let's take one step back. 12:10

Let's say that you are trying to build a memory module with x16 bit width. Do you get that? 12:10

A. Okay. 12:11

Q. Then each of the x16 device would need to be in its own rank by your definition, correct? 12:11

A. Yes, that would normally be what you would do. 12:11

Q. Okay. So in that situation, when would you be using a four 32Mbx16 device organized in supposedly four ranks versus two 64Mbx16 DRAM device organized in supposedly two ranks? 12:11

A. There would be a number of motivations to do it. One would be a pricing analysis. 12:11

Q. Okay. 12:12

A. Another would be a performance analysis based on the fact that having more ranks will typically allow you to have more pages open at a time. Those would be the two primary things that you would consider. 12:12

Q. What about power consumption? Would there be any difference? 12:12

A. So the choice is two ranks -- or four ranks of 32Mb versus two ranks. Yes, the four ranks would have lower power consumption under typical use conditions. 12:12

Q. Why is that? 12:12

A. Because the number of chips responding to any individual command would be smaller. That would be the primary reason. And the increased number of available pages would be the other reason. 12:12

Q. What do you mean by the increased number of available pages? 12:13

A. You have one page register per bank. So in the case of four 32Mbx16, you would have 16 banks of memory, with a "B," 16 bits wide, where in the case of four 64Mbx8s arranged in two ranks, you would have eight banks -- with a "B" -- with eight page registers, each 16-bit wide. So that's a 12:13

little bit lower performance in most situations and -- 12:13

(Simultaneous speakers.) 12:13

Q. Then -- 12:14

A. -- power -- 12:14

Q. Okay. Then would the 64Mbx8 and the 32Mbx16, would they have similar power consumption? 12:14

A. It depends what you mean by "similar." I think generally, in the configurations that we talked about in the last question, the 32Mbx16 would be the lower power option. But there are various trade-offs one has to look at depending on whether it's buffered or unbuffered and cost. 12:14

Q. When you say buffered and unbuffered, what do you mean? 12:14

A. You have to look at the actual loading on individual signal lines in an unbuffered device, and that may limit your options or it may limit the speed of some of your options. You have to look at the details. In a buffered device, that's less of an issue. 12:14

Q. When you say buffered, what buffer are you talking about? Data buffer? Control signal buffer? 12:15

A. Any -- any of those. You would have to analyze them all. 12:15

Q. In Perego's case are there buffers? 12:15

A. Yes, in Perego's case I believe everything is buffered. 12:15

Q. And did you perform an analysis for that buffered DRAM as to the power consumption and the performance difference for -- for a memory module with four x8 device versus a memory module with four x30 -- x16 device? 12:15

A. No. That would be an ordinary engineering task. It would depend on the -- on the very detailed specifications of the individual devices that you were using, and it would be part of any engineering implementation to do that analysis. Not to see which one's better but just to make sure that both choices are viable. 12:16

Both choices would definitely be viable under certain conditions. You'd have to look at the conditions for your particular design. 12:16

And as I mentioned, there are fundamental principles that would indicate that the x16 simply involves fewer chips and has more banks, and therefore, would generally be preferable in terms of power consumption. 12:16

Q. So we're talking about 4x4 -- let me withdraw that. 12:17

We're talking about four 32Mbx16 chip versus four 16Mbx8 chips, correct? 12:17
A. Correct. 12:17
Q. So they would have the same number of chips and banks? 12:17
A. No. I can see why that would be confusing. 12:17
The fact is, if you were to use the 64Mbx8 in a x16 configuration, you would have to use the chips in pairs for each access. So you would not get 16 banks. You would only get eight. 12:17
Q. But if you use 16Mbx16, that will be the same number of chips as when you used 32Mbx16; is that right? 12:18
A. 16Mbx16 versus 32Mbx16? 12:18
Q. No, 64Mbx16. So the last entry in Table 3. 12:18
A. It would be the same number of chips but different capacity, yes. 12:18
Q. Okay. So -- and there are more banks per chip for the 64Mbx16 than the 32Mbx16, correct? 12:18
A. In this generation, that was correct, yes. 12:18
Q. So wouldn't that mean the 64Mbx16, it would be -- actually consume less power per memory unit than the 32Mbx16? 12:19

A. Ordinarily that would be the case, but you would have to look at the details. It would depend on -- it would depend on a lot of details. 12:19
Q. Okay. So ordinarily, if you use two 64Mbx16 memory module, it will consume less power than a memory module with four 32Mbx16 devices, assuming that the module bit width is 16. 12:19
Does that sound right? 12:19
A. Again, it depends on the details, but that would ordinarily be the case or most commonly be the case. The reason one would not do that is it might cost 10 times as much at certain points in the product cycle. 12:20
Q. Okay. But once they both get to the mass production phase, the memory cost would at least be comparable, if not cheaper, for the 64Mbx16; is that right? 12:20
A. At some point that usually happens, but it's not necessarily when they both meet -- hit mass production. Because it could be that still that the yields are lower. On the -- on the higher-density device, the tooling is more expensive. At some point, historically prices have always crossed over. But it's not always at the point where they both reach mass production. 12:20

Q. Okay. And do you know the price difference per memory unit in the 2004 and 2005 time period? 12:20
A. It would have varied week to week. 12:21
Q. But do you know what the general trend was? 12:21
A. No, not off the top of my head. 12:21
Q. And ordinarily would a memory module with two 64Mbx16 memory device perform better than a memory module with four 32Mbx16 device, assuming the bit width is x16 for the memory module? 12:21
A. In the majority of cases for these generations, I believe that it would. But again, it may be cost prohibitive. 12:21
Q. Okay. We've been talking about memory modules. What is your understanding of what a memory module is? 12:22
A. In the context of these patents, it's typically a printed circuit board that has one or more memory chips soldered on it along with potentially one or more supporting components. 12:22
Q. So if you have a PCI card with memory disposed on them, are they memory modules? 12:22
A. It depends on the time frame and the concept -- context. Certainly the PCI replaced the 12:22

ISA bus. And in the early days of the ISA bus, there were certainly memory modules that went onto an ISA bus. 12:22
But by the 2004-2005 time frame, I think the intent, or the usage of that term in the '912 patent seems to be consistent with a memory module that was intended to go into a dedicated memory slot and not a general-purpose IO slot. 12:22
Q. Okay. So like by 2004-2005 time period, if a person of ordinary skill in the art at one time was talking about memory module, they are thinking about a printed circuit board that's going to be inserted into a memory slot rather than a general-purpose bus slot. 12:23
Does that sound right? 12:23
MR. CHANDLER: Objection. Form. 12:23
THE WITNESS: I think that would be the most common, but I think they would be familiar with both. 12:23
BY MS. ZHONG: 12:23
Q. I'm just asking you, when a person of ordinary skill in the art hear the word "memory module," what would they understand it to be? 12:24
A. I think they'd look for context. And in the context of the '912 patent, I think that they 12:24

are looking for something that would go into a dedicated memory slot. But in another context, they may be looking for something broader. 12:24

Q. And in what context would they understand it to be something broader? 12:24

A. There are many historical systems I can think of. The VME bus computers. The IDE bus computers in which memory modules were commonly placed in general-purpose slots. Again, I think it just depends on what the context of the system is. 12:24

Q. And when you say VME bus computers, IDE bus computers, those were old computer systems predating -- before like 2000; is that correct? 12:25

A. They were predominantly before 2000. They were still in use in 2000, but they weren't popular. 12:25

Q. Would they have been phased out by the 2007-2008 time period? 12:25

A. I don't know. They wouldn't have been common on desktops, but they survived for a long time in -- in industrial applications. 12:25

Q. '912 deals with the concept of rank multiplication, correct? 12:26

A. It does. 12:26

Q. When is rank multiplication used? 12:26

Let me withdraw and reask. 12:26

When would a person of ordinary skill in the art apply the rank multiplication concept? 12:26

A. Whenever they had any reason to use a larger number of low-density memory devices instead of a smaller number of high-density devices, or in some cases where only the devices -- where there's not a distinction in terms of density but there's a distinction in terms of availability. 12:26

Q. When you say "availability," what availability? 12:27

A. In other words, if I have two kinds of memories that have the same density. And I could potentially use one without rank multiplication and one with rank multiplication. But the one that would be used without rank multiplication isn't available in the quantities that I need. Then I could use the rank multiplication instead. 12:27

Q. So for commodity SDRAMs, the second reason for availability is less of a concern; is that correct? 12:27

A. No. Historically commodity SDRAMs have been cyclical in terms of their price and availability. So there are periodic shortages. That's one of the things that has actually driven variations in memory module implementation. 12:27

Q. And when would you use lower-density memory devices instead of high-density memory devices? 12:28

A. There could be a number of reasons. But primarily it's either because you get a lower cost per unit or you have improved availability. 12:28

Q. When you say "lower cost per unit," what's a unit, memory unit? 12:28

A. Yeah, unit of storage. 12:28

Q. And when wouldn't you use rank multiplication? 12:29

A. There's a number of considerations. If you wanted to use a small number of memory devices and that was your cheapest approach, that could be a reason not to use rank multiplication. 12:29

If you wanted to build a very simple device that had the smallest amount of additional logic on the DIMM, that could be motivation. 12:29

But again, usually the motivation is total cost per unit memory, which can change over time. 12:30

So often in the late stages of a generation of memory devices, you can build a complete DIMM with one or two or four or eight devices in a single rank cheaply. And at that point, rank multiplication may not solve the problem for certain customers. 12:30

Q. But if you have -- but if there's only a single device per rank, would cost still be a consideration? 12:30

A. Could be. So, for example, if I'm -- if I'm making computers for 3rd graders and I can have them run the software using a one-rank, one-device memory system, that could be very cheap and effective. 12:31

Q. Why would you even have a memory module if there's only a single device per rank? Can't you just connect the DRAM directly to the memory system? 12:31

A. You can, but there are many reasons why you may not want to. One of those may be you want to repurpose the same computer system for different markets. So you may want to have a version with more memory that you sell to 6th graders than the one that you sell to 3rd graders. 12:32

Another version -- reason may be, as you said, memory tends to be a commodity so you don't want to commit to a particular chip at the time that you're making the boards. Instead, at the time that you sell the computer out the door, you want to purchase your memory on a module just in time since you don't have the carrying costs to that memory. 12:32

Those are some of the common reasons. 12:32

MS. ZHONG: Do you want to take a lunch break right now? 12:32
THE WITNESS: We can do that. 12:32
MS. ZHONG: Do you want to take an hour? 12:33
MR. CHANDLER: That's fine. 12:33
(Whereupon a luncheon recess was had.)
12:33 (Off record: p.m.) 12:33
(On record: 1:30 p.m.) 12:33

Q. You are familiar with this document, correct? 01:32
A. Yes. 01:32
Q. Can you please take a look at paragraph 10 through 19. 01:32
A. Okay. 01:32
Q. Do you see there's a Table 1 in paragraph 11? 01:33
A. Yes. 01:33
Q. In Table 1, follows 2, 3, 4 and 5 have the headings CS0, CS1, An+1 and Control. 01:33
Do you see that? 01:33
A. I do. 01:33
Q. Are those input signals received from the memory system in order to select the rank? 01:33
A. A subset of them are in some cases. 01:34
Q. Are those the signals that's received by the ASIC depicted in Figure 1? 01:34
A. They appear to be with the distinction that in Table 1 there's only a single control signal. And in the text it explains that only a single control signal is required. 01:34
Q. What do you mean by only a single control signal is required? 01:34
A. Let me see if I can find that. 01:35

Wednesday, January 4, 2023 01:30
1:30 p.m. 01:30
01:30
MS. ZHONG: We can go back on the record. 01:30
EXAMINATION (resumed) 01:30
BY MS. ZHONG: 01:31
Q. Dr. Wolfe, can you pull up Exhibit 1004 {sic}, which is U.S. Provisional Application 60/588244. 01:31
(Exhibit 1005 was marked for identification and attached hereto.) 01:31
BY MS. ZHONG: 01:31
Q. Do you have that document? 01:31
A. Give me the exhibit again. 01:31
Q. Exhibit 1005. Exhibit 1005. 01:31
MR. CHANDLER: Can we pause for a moment? My colleague got kicked out from the Zoom and he's coming back in. 01:31
MS. ZHONG: So let's go off the record while waiting for him then. 01:31
(Brief pause in proceedings.) 01:31
BY MS. ZHONG: 01:32
Q. Do you have Exhibit 1005, Dr. Wolfe? 01:32
A. Yes. 01:32

Paragraph 10, it says at least one control signal. 01:35
Q. Okay. If you look at paragraph 11, note 4, that describes what the control in Table 1 refers to; is that correct? 01:35
A. Yes. 01:35
Q. Okay. So in Table 1, the control refers to a number of control signals that define operations such as refresh, precharge, and other operations, correct? 01:35
A. That is what note 4 says. 01:35
Q. And what would those control signals be if the DRAM is JEDEC compliant on the DRAM -- 01:35
THE REPORTER: I'm sorry. "If the DRAM is"... 01:36
BY MS. ZHONG: 01:36
Q. And what would those control signals be if the DRAM is a JEDEC compliant DRAM device? 01:36
A. Well, there are many different kinds of JEDEC compliant DRAM devices, but a typical example could be RAS, CAS, and write enable. 01:36
Q. Does it need to have chip select signal? 01:36
A. No, because the chip select signals are separately defined CS0 and CS1. 01:37
Q. Okay. And for read and write operation, 01:37

does it also need to -- does bank address information also need to be provided? 01:37
A. Again, there's nothing that needs to be provided other than something that performs the function. But I would not expect bank address to be provided. I don't -- I'm not aware right now of a situation where bank address defines operation such as refresh and precharge. 01:37
Q. So you mean -- what about a read and a write? 01:37
A. What about them? 01:37
Q. So are read and write operation, do bank addresses need to be provided in order to define the operation? 01:38
A. They may need to be provided to the memory chip in order to identify where the operation should take place, but they don't need to be provided to the ASIC decoder that's shown in Figure 1. 01:38
Q. The ASIC decoder says the control involves control signals that define operations, correct? 01:38
A. No, that's what Table 1 says. 01:38
Q. And paragraph 19 says, "The 'Control' column of Table 1 represents the various commands that a DRAM device can execute, examples of which include, but are not limited to, activation, read, 01:38

write, precharge, and refresh," correct? 01:39
A. Correct. 01:39
Q. And we discussed earlier that for a JEDEC compliant SDRAM, the command for a read and write operation and activation would include bank address signals, correct? 01:39
A. We're talking about different things here. 01:39
So, one -- there's nothing in Figure 1 that indicates that that's a JEDEC compliant DRAM. 01:39
But even so, the discussions we had before were about what the DIMM module would receive, not what an ASIC decoder on a DIMM module would receive. And those are two different issues. 01:39
Q. Okay. I'm just asking the control information of the command signals that a DRAM -- let me withdraw and ask. 01:39
The commands that a DRAM device can execute includes a read operation command, correct? 01:40
A. It would depend what kind of DRAM device. 01:40
But that would be true for most DRAM devices is that there's some type of a read operation. 01:40
Q. Okay. So let's say, since you are only citing the JEDEC compliant DRAM devices, for those DRAM devices, the commands for a read and write operation includes bank address information, 01:40

correct? 01:40
A. Let's be clear. I'm not only citing JEDEC compliant DRAM devices. And where I do cite them, it's to illustrate the obviousness issues with respect to particular references. The -- I would not rely on the JEDEC compliant DRAM specification as a way to understand what's disclosed in Exhibit 1005. 01:40
Q. The DRAMs in Exhibit 1005 are to be used with a general personal computer, correct? 01:41
A. Yes. 01:41
Q. And we agree that a JEDEC compliant DDR or DDR2 DRAM device in order to execute -- let's withdraw -- let me withdraw and reask. 01:41
So the commands are for a read operation for a DRAM device that is compliant with JEDEC standard would include bank address information; is that correct? 01:42
A. As I said, there are many, many JEDEC standards. I can't generalize about all of them. 01:42
Q. Okay. The JEDEC standards you cited. 01:42
A. I would not consider the bank addresses to be part of the command, no. They are supplied along with a command, but in the -- for example, Exhibit 1029, when I look at a command like the bank 01:42

activate command, the bank activate command is issued by holding CAS bar and write enable bar high with chip select bar and RAS bar low at the rising edge of the clock. 01:43
Q. And bank address signal is supplied with those commands in order to execute the bank activation? 01:43
A. It is supplied to the DRAM chip along with the command. It is neither part of the command nor is it something that necessarily would go through a separate logic circuit. 01:43
Q. Okay. And I think you mentioned earlier that it is not necessary for the larger component to actually receive the bank address signal. All it requires for a JEDEC compliant SDRAM is for the DRAM itself to receive the bank address; is that correct? 01:44
A. In order to use a DRAM chip such as the kind that's described in Exhibit 1029, that is correct. 01:44
Q. Okay. So the bank address signal need not be received by a larger element? 01:44
A. Not in every utilization of a DDR2 device, no. 01:44
Q. Okay. And so is there anything in Perego actually mentions the bank address signal being 01:44

passed to the buffer address -- buffer device? 01:45
A. I believe all the signals that are 01:45
communicated in Perego from the host are passed 01:45
through buffer devices. 01:45
Q. Does Perego actually mention a bank 01:45
address in particular? 01:45
A. It mentions memories that have banks. And 01:45
it mentions specific memory types like DDR that 01:46
would -- a person of ordinary skill would understand 01:46
has a bank address. 01:46
Q. So if you mention DDR or DDR2, does that 01:46
necessarily mean a JEDEC compliant DDR or the DDR2 01:46
device? 01:46
A. No, not always. But it would certainly 01:46
cause a person of ordinary skill to find the use of 01:46
one obvious. 01:46
Q. So in Figure number 1, how would the bank 01:47
-- (indiscernible.) 01:47
THE REPORTER: I'm sorry, Counsel. 01:47
Counsel, can you speak more to your right? We're 01:47
losing you. Thank you. 01:47
BY MS. ZHONG: 01:47
Q. So in Figure number 1, if the DRAM device 01:47
is a DDR or DDR2 JEDEC compliant device, how would 01:47
the bank address information be provided to that 01:47

DRAM device? 01:47
A. Figure 1 of Perego? 01:47
Q. No, Figure 4, Exhibit 1005. 01:48
A. So, again, there's no mention of JEDEC 01:48
standard devices. But if one were to choose to 01:48
implement Figure 1 of 1005 with DDR2 JEDEC compliant 01:48
devices like in Exhibit 1029, they would have to 01:48
consult Exhibit 1029 to figure out how to connect 01:48
them up. 01:48
And presumably they would simply take the 01:48
bank address signals directly from the host bus and 01:48
connect them directly to each memory device. That 01:48
would certainly be the simplest way to implement it. 01:48
Q. Would the bank address information be 01:49
required to operate a JEDEC compliant DDR or DDR2 01:49
device? 01:49
A. I don't know that I could look -- I'd have 01:50
to think about it. 01:50
No, I mean, it's not required in all 01:50
circumstances. But if one were to build an ordinary 01:50
PC memory module, one would -- typically at that 01:50
time, the simplest thing to do would be to connect 01:50
the bank address signals directly from each memory 01:50
device to the host computer memory controller. 01:50
Q. Even when you have a register? 01:50

A. Well, it depends why you have a register. 01:50
In this particular case, the register is quite 01:50
limited and is only used for a subset of address 01:50
signals. 01:50
Q. What about on the -- (indiscernible.) 01:50
THE REPORTER: I'm sorry? 01:51
THE WITNESS: What about on the what? 01:51
BY MS. ZHONG: 01:51
Q. On the (indiscernible) -- 01:51
THE REPORTER: I don't -- 01:51
MS. ZHONG: It's on Exhibit 1032. 01:51
MR. CHANDLER: Are you saying registered 01:51
DIMM, the letter R DIMM? 01:51
MS. ZHONG: Yes. 01:51
MR. CHANDLER: Okay. 01:51
THE WITNESS: And what's the question 01:51
about the registered DIMM? 01:51
BY MS. ZHONG: 01:51
Q. Okay. So for the DIMM that's described in 01:51
Exhibit 1032 -- 01:51
A. Yes. 01:51
Q. -- where are the advance signals sent? 01:51
A. In the DIMMs that are described in 01:51
Exhibit 1032, the bank signals from the host 01:51
computer are registered. And then the registered 01:51

copies of those signals are sent to each of the 01:52
SDRAM chips. 01:52
Q. For the registered DIMM shown in 01:52
Exhibit 1032, does that register have any logic 01:52
function? 01:52
A. Not in the way I would normally use that 01:52
term, no. It's simply register. 01:52
Q. How would you use -- what's your 01:52
definition of a logic element? 01:52
A. Well, again, it depends on context. But 01:52
in the context of something like the '912 patent or 01:52
Exhibit 1005, I would think that a logic element 01:52
performs logic functions by combining multiple 01:52
signals for the purpose of incorporating a logic 01:53
equation and not simply delaying a signal. 01:53
Q. Okay. And what is sequential logic? 01:53
A. What is sequential logic? 01:53
Q. Yes. 01:53
A. Sequential logic -- again, you have to 01:53
look at the context. Normally it describes a 01:53
combination of logic functions and registers. 01:53
Q. What do you mean by "It describes a 01:53
combination of logic functions and registers"? 01:53
A. I don't know how to simplify this down to 01:53
a single statement. It takes us hours or days to 01:53

explain it to students. 01:54
But sequential logic implements what we 01:54
call state machines, which are time-variant logic 01:54
functions that can perform different logic equations 01:54
at different points in time based on the storage of 01:54
what we call state partial results. 01:54
Q. Okay. So in order to implement a 01:54
sequential logic, normally you would need to have 01:54
both electrical elements that execute the logic 01:54
function and also storage elements that store the 01:54
state of the device? 01:54
Does that sound correct? 01:54
A. It would normally -- 01:54
MR. CHANDLER: Objection. Form. Also 01:54
incomplete hypothetical. 01:54
THE WITNESS: Generally, to perform a 01:55
sequential logic function the way that I've defined 01:55
it, you would need both state storage in the form of 01:55
a register or an equivalent, plus some what we call 01:55
combinational logic functions. 01:55
That doesn't mean that the same signals 01:55
are provided to both, or it doesn't mean that they 01:55
work in any particular way, but they would both 01:55
somehow be present. 01:55

BY MS. ZHONG: 01:55
Q. Okay. What is combinatorial logic? 01:55
A. Combinatorial logic is logic that does not 01:55
store results, basically. 01:55
Q. So basically it's -- it generally only 01:55
refers to the logic operation without the storage 01:55
unit? 01:55
A. Correct. Generally, a change in input 01:55
would be reflected as a change in output and a clock 01:55
is not required. 01:55
Again, you know, it gets more complicated 01:55
than that when you dig into the details, but that's 01:55
kind of a -- a very high-level overview. 01:56
Q. Okay. Is that something a POSITA would 01:56
have understood in 2004 and 2005 as to what 01:56
sequential logic and combinatorial logic is? 01:56
A. They would have understood the textbook 01:56
definitions, yes. 01:56
Q. You said that the -- why don't you pull up 01:56
Exhibit 1009, the patent ending with '436. 01:56
A. Okay. 01:57
(Exhibit 1009 was previously 01:57
marked for identification and 01:57
attached hereto.) 01:57
BY MS. ZHONG: 01:57

Q. Is it your opinion that '436 patent does 01:57
not describe the solution for the back-to-back 01:57
adjacent reads with cross memory device boundary? 01:57
A. It does not. 01:57
Q. And what is a back-to-back adjacent read 01:58
command issue that we're talking about? 01:58
A. That when commonly available protocols at 01:58
the time, such as the DDR and DDR2 protocols, were 01:58
used together with a very simple rank multiplication 01:58
scheme, there was a problem when a read command went 01:58
to one rank and a subsequent read command went to 01:58
another rank in that certain signals were driven for 01:58
a longer time period than it would take to simply 01:58
respond or to simply provide the data in response; 01:58
that there were preambles and postambles in the 01:58
response signals. 01:59
And if one simply connected up two ranks 01:59
to be sequentially accessed, those signals could 01:59
conflict with each other. And some mechanism had to 01:59
be introduced in order to distinguish those signals 01:59
or to block one of those signals so that there would 01:59
be no interference. 01:59
Q. So it's -- is it essentially a DQS bus 01:59
conflict situation then? 01:59
A. Did you say d2s? 01:59

Q. DQS, Q as in quiet. 01:59
A. Let me look at the actual signal name 01:59
there, yes. 01:59
That's -- that's the -- the significant 01:59
one. There's DQS and DQS bar in some generations. 01:59
And that's where the preamble and postambles would 02:00
exist. 02:00
And one of them -- either the timing needs 02:00
to be adjusted between the two ranks or one of those 02:00
DQS response signals to a read needs to be blocked 02:00
or they need to be combined. 02:00
Q. Okay. So basically we're talking about a 02:00
DQS bus conflict situation, how to resolve it? 02:00
A. That's the most common situation that 02:00
would come up, yes. 02:00
Q. Okay. Let's see. 02:00
Can you pull up Exhibit 1030, page 19. 02:00
A. Yes. 02:01
Q. And you reference the Figure 8 in your 02:01
discussion of the read -- the back-to-back read 02:01
situation. 02:01
Is Figure 8 depicting a back-to-back read 02:01
that's across rank boundaries? 02:01
A. So the -- the -- the simplest 02:01
interpretation of Figure 8 is that it represents 02:01